Ultra-Low Power Pulse-Triggered CNTFET-Based Flip-Flop

فلیپ فلاپ براساس سی ان تی اف ای تی با تحریک پالسی بسیار کم مصرف

Ahmad Karimi, Abdalhossein Rezai, and Mohammad Mahdi Hajhashemkhani

***Abstract*—Reducing the power consumption and scaling the devices are the important concerns of today's electronics. Flip-Flop (FF) is one of the basic elements in electronic devices. Thus, the performance of the electronic devices is improved by improving these qualities in the FFs. In this paper, a novel pulse-triggered CNTFET-based D-Flip-Flop structure is proposed. This structure utilizes signal feed through technique to reduce the "0" to "1" transition,whichrequiresonlyoneCNTFET.Moreover,thedischargi ng path is optimized to reduce the delay time for "1" to "0" transition by using only two CNTFETs. The novel structure is simulated in Hspice using Stanford model. The output results prove that the performanceoftheproposedstructureisimprovedgreatlyinterms of power consumption, D-to-Q delay, the power-delay product, and the number of required transistors in comparison with other pulse-triggered Flip-Flop structures.**

***Index Terms*—Flip-flops, CNTFET, PDP, nanotechnology, pulse triggered, low power design, signal feed through technique.**

I. Introduction

IN THE last few decades, scientists have tried to optimize the performance of electronic devices especially two important qualities of them: 1) scaling devices based on Moore's law, and 2) reducing the power consumptions [1]–[4]. On the other hand, Flip-Flop (FF) is considered as one of the basic elements in VLSIcircuits[5].Therefore,theperformanceofmanyelectronic devices can be improved by improving the characteristics of the FFs. The Pulse triggered Flip-Flops (P-FFs) are usually utilized in high-speed applications. This is due to their single latchstructure, which attractsmoreattention incomparison with conventional Master-slave FF (M-FF) [6]–[11]. Amongst these designs,theP-FFshaveshownthemostpromisingapplicantsfor low-power consumption and scaling [12]. Therefore, the P-FF is investigated in this paper.

Most of the P-FF designs are based on Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET). Different method of improvements based on CMOS technology is presented in [7]–[11], [13], [14].

Something that all of these researches has in common is that they reduced the number of required transistors to improve the size and the power efficiency of FFs. In [10], a method is utilized that requires 25 transistors. Some of them are responsible for generating the necessary pulse and others are required to accumulate the output. In [14], the number of transistors is reduced to 24 transistors. In [13] the number of transistors is reduced to 19 transistors because of the utilized pulse generator. In [7], the leakage power was reduced thus reducing the power consumption, which is based on the transmission gate utilized in the input data. This design has shown a great improvement in case of power efficiency, but the designed pulse generator in this paper requires a very delicate sizing of the transistors. Although all of these designs and structures have helped to improve FFs characteristics, but they have to follow the limitation of CMOS technology. Recently, some ideas have been proposed to replace CMOS technology, such as Silicon-On-Insulator Field Effect Transistors (SOIFETs) and Carbon Nano Tube Field Effect Transistors (CNTFETs) [2], [15]–[17]. The best technology till this day is considered to be CNTFET technology [1]–[3], [18]–[24].

Inthispaper,anewstructureisproposedtodesignaCNTFETbase d FF. The proposed structure is based on an explicit-pulsetriggered Signal Feed Through technique Flip-Flop (SFT-FF). The proposed structure has the following characteristics:

a) It utilizes signal feed through scheme technique to reducethe "0" to "1" transition.
b) It optimizes the discharging path to reduce the delay timefor "1" to "0" transition.
c) Itspulsegeneratordoesnotdependonthetransistor'ssize.
d) It uses the best combination of CNTFET parameters specially the number of CNTs and Diameter of utilized CNTs (D_{CNT}).

The designed CNTFET-based FF is simulated in HSpice. The results show that the proposed CNTFET-based FF structure has improvements compared to other FF structures.

This paper is organized as follows: Section II gives a brief overview of CNT modeling, Flip-Flops and the proposed design structure. Section III shows the simulation results and comparisons, and finally, Section IV concludes this paper.

II. Approach

A. A Brief on CNTFET Features

The CNTFET structure, which is used in the proposed design in this paper, is shown in Fig. 1.

Manuscript received December 9, 2018; revised February 15, 2019 and April 18, 2019; accepted July 11, 2019. Date of publication July 22, 2019; date of current version July 30, 2019. The review of this paper was arranged by Associate Editor M. T. Cole. *(Corresponding author: Abdalhossein Rezai.)* The authors are with the ACECR Institute of Higher Education, Isfahan 84175-443, Iran (e-mail: ahmadkarimi260@gmail.com; rezaie@acecr.ac.ir; Mm_hhkh@gmail.com).

Digital Object Identifier 10.1109/TNANO.2019.2929233

This structure helps to visualize the CNTFET structure and would be helpful to understand the features of this device.

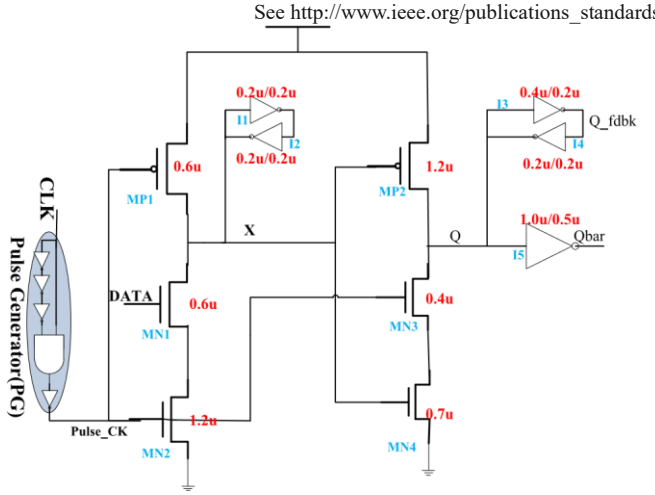


Fig. 2. The DCO P-FF structure used in [10].

The CNTFET current equation is shown as follows [22]–[24]:

$$I_{CNTFET} \approx \frac{N g_{CNT}\,(V_{DD} V_{th})}{1 + g_{CNT} L \rho_S} \quad (1)$$

Where L and ρ_S denote the CNT length and the source resistance per unit length of the CNT, respectively. The g_{CNT} denotes the transconductance per CNT.

B. Pulse-Triggered Flip-Flops

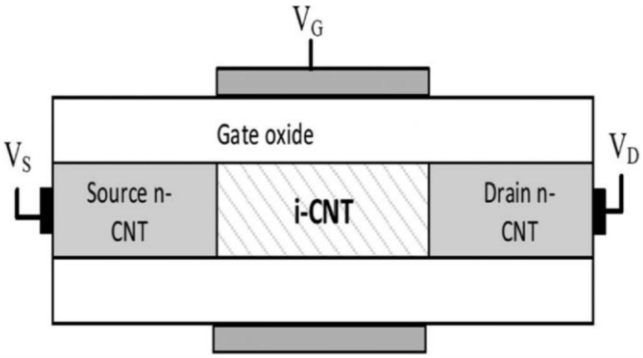


Fig. 1. The utilized CNTFET structure [1].

There have been many proposed designs for the Flip-Flops, but the most power economical kind of these devices is the explicit P-FF [7]. Some of these P-FF designs are shown in Figs. 2–4 [10], [13], [14]. Fig. 2 shows a Data-Close-to-Output (DCO) P-FF [10].

The critical path to change the logic value of output Q from "0" to "1", has three transistors in its structure. Moreover, the Power-Delay Product (PDP) of this design would not be suitable for low-power applications due to the complexity of the circuit model.

Fig.3showsanotherdesignstructurenamedModifiedHybrid Latch Flip-Flop (MHLFF) [13].

The advantage of this design is in its utilized simple circuit. The number of required transistors for this design is reduced. Thus, it can improve the power consumption of FF, but this

Fig. 3. The MHLFF structure used in [13].

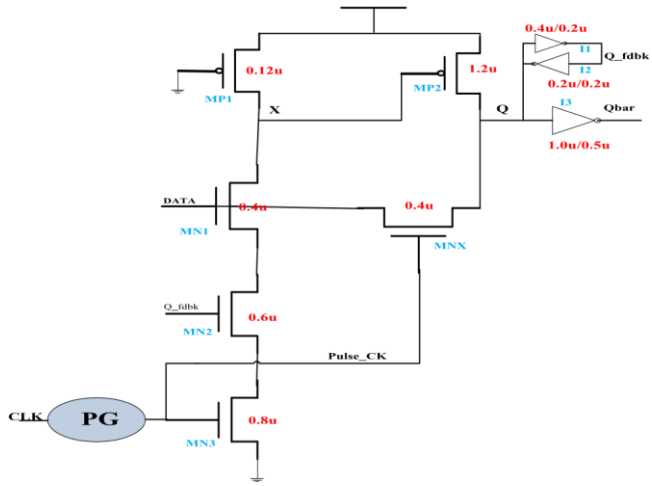
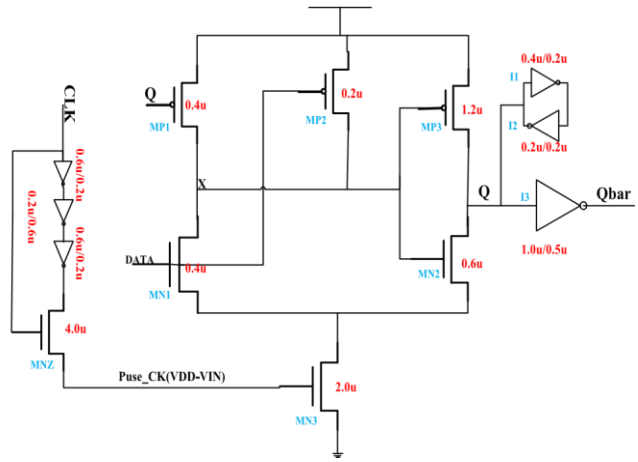


Fig. 4. Pulse-triggered Flip-Flop based on the SFT scheme in [14].

design suffers from a long delay. It is because node X is not predischargedandinsomecases,itsvaluewouldbefloat.Moreover , it faces a longer delay when the output logic value transits from "0" to "1".



The design shown in Fig. 4, which is proposed in [14], has a lower delay when the output Q is transiting from "0" to "1" by adding MNx between the input and the output.

This design has shown the most promising output amongst other designs. Although this design has advantages, its performance can be improved as described later.

Our proposed model to improve the performance of the D-FF is shown in Fig. 5.

The proposed structure is based on CNTFET technology. The main advantage of this circuit besides reducing the number

of transistors is the utilization of CNTFET in its structure. It should be noted that the CNTFET parameters such as Diameter (D_{CNT}) and the number of CNTs can affect the CNTFET output [1]–[3], [25], [26]. In our previous works [1]–[3], different combination of CNTFET's parameters were considered to gather the best possible outcome with the least possible power consumption. The numbers provided besides each CNTFET in figure 5, are the

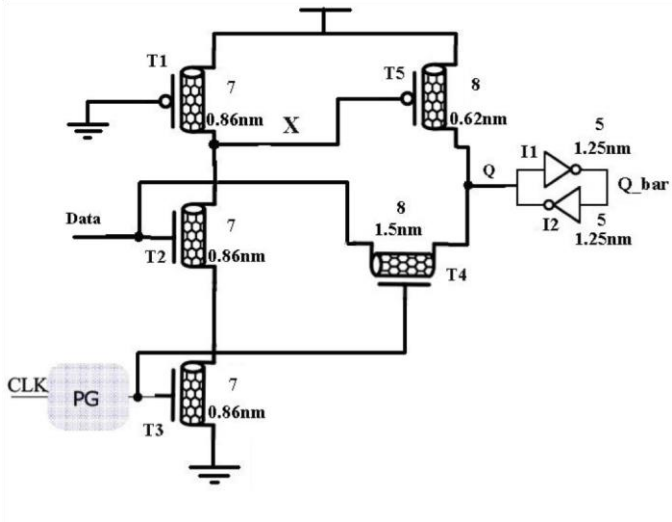


Fig. 5. The proposed structure for the D-FF.

number of CNTs (the upper digit) and their diameter (the lower number). Also the chosen t_{oxide} and CNT's length for all the CNTFETs are 5 nm and 16 nm, respectively. These CNTFETs are based on the results gathered from [1]–[3], [25], [26], so that not only they can act as a D-FF correctly, but also the total power consumption of the device would be reduced as much as possible.

The proposed structure discharges node X through two NCNTFETs.TwoinvertersI1andI2areusedtoholdthevalueof nodeQwhentheclocksignalisloworthe flopisnottransparent. The CNTFET T4 and its size are calculated to change the output in response to the changes in data and CLK. When the data and CLK are equivalent to logic values of 1, the CNTFET T5 is turned ON. Therefore, node Q is connected directly to the voltage source and its logic value would be equivalent to 1. It should be noted that in this structure, the number of CNTFETs has been reduced. Omitting certain CNTFETs could result in lower current and power consumption. The unique structure and the characteristics of CNTFET technology helped to improve the power performances of the proposed structure further. In addition, the required layout area could also be reduced due to the usage of CNTFETs. As it is shown in Fig. 5, the input data only has to pass through one CNTFET (T4). Therefore, it reduces the delay time of D-FF.

III. Simulation and Discussion

The proposed structure for the D-FF is simulated in Hspice. There are many different models that have been proposed for the simulationofCNTFETs[1],[2],[7],[14],[25],[27],whichhave advantagesanddisadvantages.Here,duetothemanyadvantages of the Stanford model, such as simplicity and required accuracy of this model toward others, it has been chosen for the simulations [27]. The circumstances and the simulation's properties are the same as the simulations' properties in [14], [7]. The 1.0 V power supply is utilized as an operating condition that makes the proposed structure suitable for low power applications. This design uses 21 CNTFETs in its structure. The results are shown

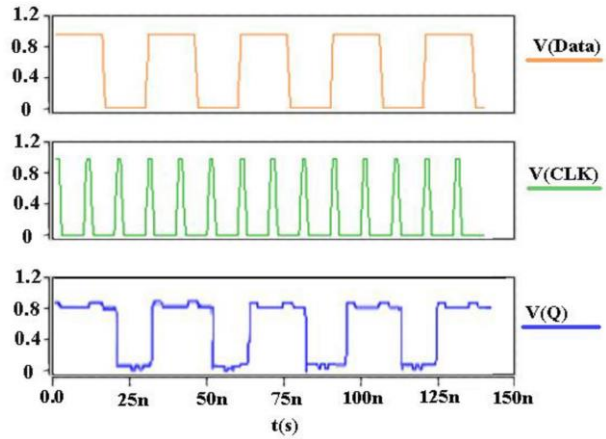


Fig. 6. The simulation results for the proposed structure.

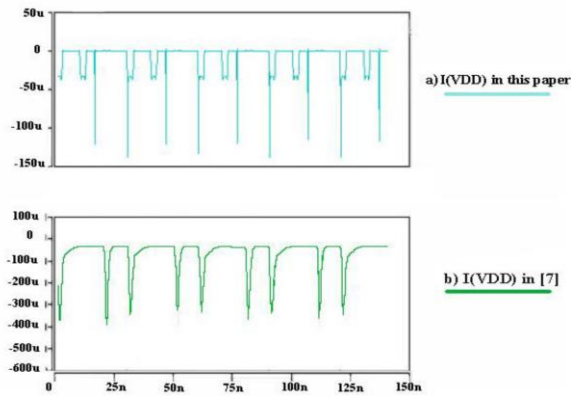


Fig. 7. The D-FF current comparison (a) in the proposed design and (b) in the ULPFF [7].

inFig.6.Theseresultsshowtheusefulnessoftheproposed D-FF structure. The current consumption of the Ultra-Low Power Flip Flop (ULPFF) [7] and the proposed design are shown in Fig. 7.

Basedonoursimulationresults,whichareshowninFig.6and Fig. 7, the FF current is reduced by about 3 times in comparison with that reported in [7]. Although this simulation is done so that the proposed FF output could be compared to the previous ones, the required voltage to drive CNTFETs and get results is very low.ThisisduetothefactthatCNTFETsareturnedONandOFF

withlowvoltages.So,thesevoltagescouldbereduced.Thus,the power dissipation of the proposed FF would be reduced as well. Tables I and II show this system functionality in comparison with similar P-FF designs. The flip flops utilized for comparison are Conditional Discharge Flip Flop (CDFF) [29], Transmission Gate master–slave-based FF (TGFF) [34], Adaptive-Couplingconfigured FF (ACFF) [8], Data-Close-to-Output (DCO) P-FF [31], Modified Hybrid Latch Flip-Flop (MHLFF) [13], Signal Feed Through technique FF (SFT-FF) [14], Ultra Low Power FF (ULPFF) [7], and FINFET Transmission Gate FF (FINFET TGFF) [28].

Based on the results shown in these tables, the power consumption of the proposed D-FF is reduced in different switching activities (100% −50% −25% −12.5% −0%) in comparison with other D-FF designs. The power consumption is reduced by about 90% in comparison with SFT-FF [14] in 50% activity. The proposed design shows an improvement by about 90% in comparison with [7] for 50% activity. The proposed structure improvement is shown in its PDP at 25% activity where this factor is optimized by about 95% and 92% in comparison with its former best Pulse triggered FF named SFT-FF in [14] and ULPFF in [7]. It should be noted that the results that provided in [14] is based on fabrication model. So, the readers should notice this in comparison. Moreover, in Table II the proposed structure is compared with FINFET-based TGFF [28]. It was shown that this FINFET-based FF has the best result amongst other pulse triggered Flip Flops. These comparison results show 80% improvement in case of PDP. The average power is also improved by about 80%.

Fig.8-ashowsthePDPfortheproposeddesignunderdifferent data switching activity. Fig. 8-b shows processors corner at 25% data switching activity. The conditions for this performance are as follows: SS = 0.8 V/125 °C, TT = 1 V/25 °C, FF = 1.2 V/ –40 °C, SF = 1 V/25 °C, and FS = 1 V/25 °C. The load capacitanceutilizedintheoutputisbyabout1fF,whichisalmost equivalent to a CNTFET fan-out-of 6 FOT6 [22], [30]. It should be noted that these circumstances are based on [7], [22], [24], [30].

These comparisons show that the power consumption of the proposed design is improved. The delay time to change the outputlogicstatefrom“0”to“1”and“1”to“0”arealsoreduced. The comparison for the average power in each case shows a great deal of improvement with former FFs. This improvement comparison with SFT-FF and ULPFF at 50% data switching activity is by about 90% and 88%, respectively. Moreover, this improvementreachesbyabout90%indifferentprocessorcorner in comparison with designs in [7], [14].

Note that Hold time (H), Setup time (U), the power delay performances of these parameters and C-to-Q delay are important timingparametersoftheflip-flops.Theseparametersaredefined as follows [7], [14]:

TABLE I

به جداول زیر دقت فرمایید

FEATURE COMPARISON OF DIFFERENT FFS

FF Design	SDFF [9]	ACFF [8]	MHLFF [13]	ep-DCO[31]	ep-SFF [32]	TGFF [33]	SFTFF [14]	ULPFF [7]	FINFET TGFF [28]	Proposed
Number of transistors	25	22	19	28	24	22	24	17	22	21
Setup time (ps)	-26	112	1.5	−83.8	-73.2	67.3	-85.7	-84.2	67.3	-80
Hold time (ps)	55.3	−60.9	95.7	110	137.1	−45.3	120.1	119.01	-45.3	118.2
Minimum D-to-Q delay (ps)	132.5	284.5	173.8	118.9	136.8	271.4	109.1	90.17	271.4	85.17
Average power (0% all-0) µW	11.98	7.55	16.75	16.96	18.10	16.70	16.17	12.07	3.147	0.288
Average power (0% all-1) µW	26.72	7.45	16.75	29.70	18.60	15.54	16.06	12.76	3.04	0.250
Average power (12.5% activity) µW	20.02	10.40	18.53	24.03	19.82	18.33	17.89	13.11	2.98	0.267
Average power (25% activity) µW	21.22	13.29	20.32	25.26	21.28	20.39	19.52	15.95	2.87	0.276
Average power (50% activity) µW	24.73	20.11	24.23	28.72	24.57	25.13	23.43	18.46	2.94	0.297
Average power (100% activity) µW	30.69	33.06	31.82	34.41	31.14	34.18	30.09	24.15	3.66	0.352
Optimal PDP (25% activity) pJ	2.84	3.78	3.58	3.03	2.91	5.54	2.13	1.58	0.126	0.0235

H: Hold time that is evaluated under the worst conditions. It is the minimum required time to hold data signal constant after the rising edge of the clock [14].

U: Setup time that is also evaluated under worst conditions. It is the minimum required time, which will guaranty the change of output Q, between a rising edge of the clock and a data change [34], [35]. This change takes place when the clock pulse width is sufficient to equalize the value of Data and output [7].

Note that the optimal timing of this device is based on the optimization of PDP_{DQ} rather than just D-to-Q. Fig. 9 shows this device simulation results for PDP vs setup time curve and C-to-Q vs hold time curve.

Based on the simulation results that are shown in Fig. 9-a, whenthesetuptimeisnegative,theminimumPDPvalueusually occurs. The proposed structure's PDP is very low.

A sufficient setup time must be applied to measure the hold time. It should be noted that when the slop of C-to-Q delay vs Hold time curve is equal to −1, the hold time is computed [23]. Fig.9-bshowstheresultofthiscomparison.TheMHLFF,TGFF, and ACFF have negative setup times. Therefore, the Hold time would also be pushed accordingly. As they would appear in the leftmostsideofthisplot,theyarenotincluded inthecomparison of C to Q vs Hold time.

Another important simulation that can help to evaluate the proposed design is the Monte Carlo simulation. This standard

deviationforthetransistorsizevariationis5%oftransistorwidth [27].InthecaseofCNTFETbychangingthediameterofaCNT, thissimulationcanbedone.In[1]–[3],thevariationoflengthand

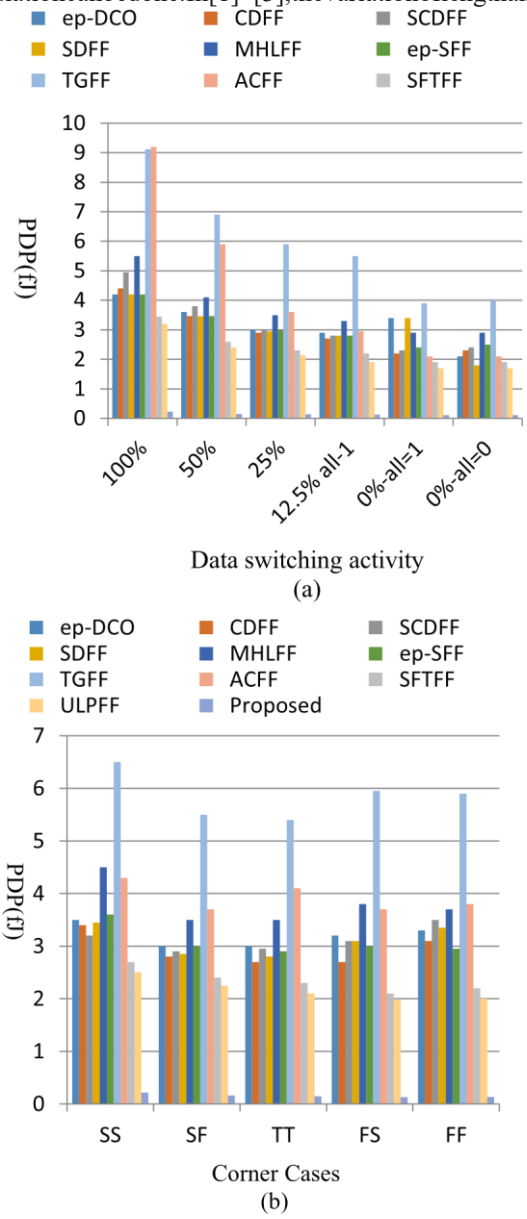


Fig.8. ThePDPin(a)Differentdataswitchingactivity.(b)Differentprocessor corners at 25% data switching activity.

diameter is discussed thoroughly. The output result is provided in Fig. 10.

As it is shown in Fig. 10, the performance of the proposed device is greatly improved in comparison with the former designs. The power consumption is decreased to nearly 1^{nw} that shows about 90% improvement in comparison with [14]. The optimum D-to-Q delay is 85.17 (pS), which happens in the FF process corner of this device.

The only limitation in CNTFETs scaling is the CNT length. Thus, the layout area of the proposed structure shows a great improvement in comparison with other designs. Based on the results shown in Tables I and II, the proposed Flip-Flop structure is a promising candidate to be used in low-power applications.

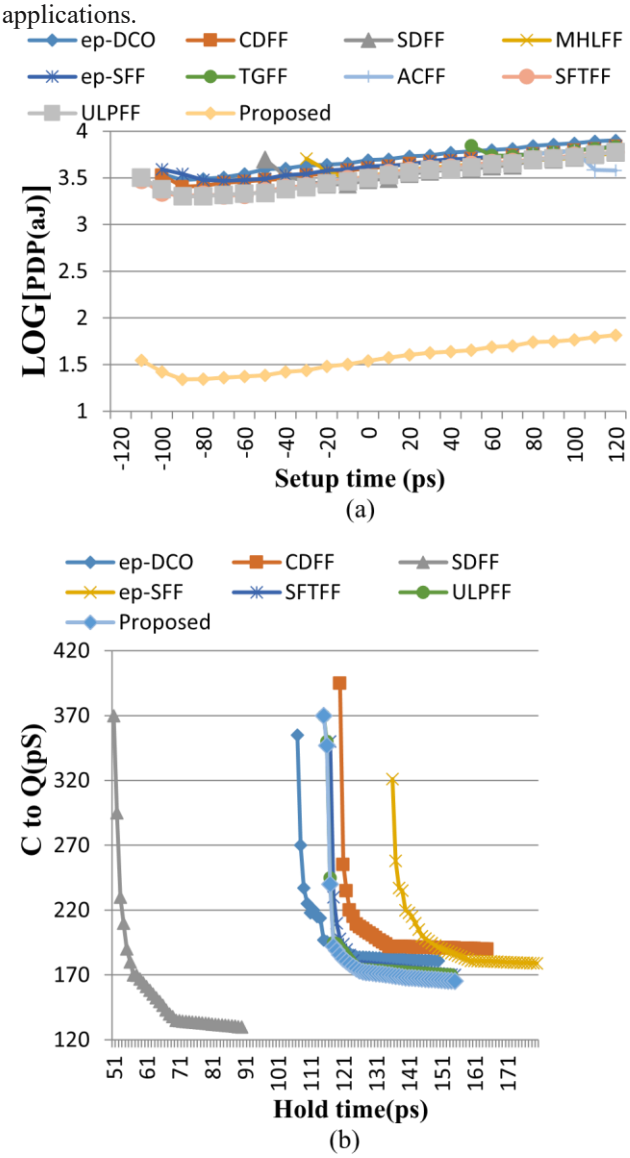


Fig. 9. The timing parameters (a) The PDP_{DQ} vs Setup time. (b) C-to-Q delay vs hold time.

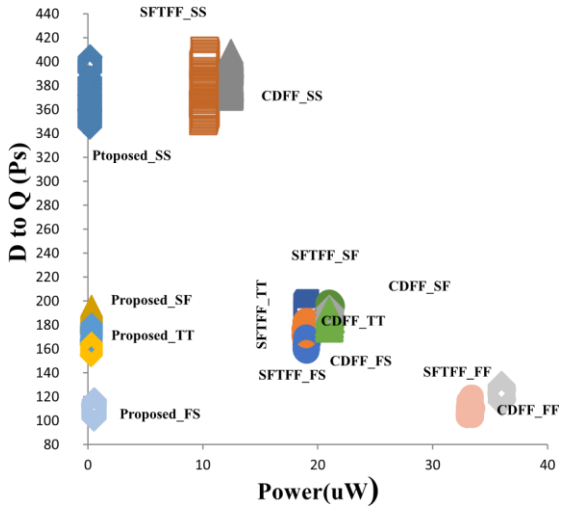


Fig. 10. The Monte Carlo simulation results.

In addition, another important quality of this structure is that it can be scaled to lower sizes.

IV. Conclusions

Flip-Flop is considered as one of the basic elements in VLSI circuits. Therefore, FFs' delay and power consumption are two important concerns of today's electronics. In this paper, a novel structure was proposed for the pulse-triggered CNTFET-based Flip-Flop. In the proposed structure, the Stanford CNTFET model [27] is utilized. The proposed FF structure was simulated using Hspice. Based on our simulation results, the proposed structure has an advantage in terms of the PDP in comparison with other pulse-triggered Flip-Flops. This comparison showed that the average power consumption at different data switching activity was improved by about 80% and 78% in comparison with SFT-FF [14] and ULPFF [7], respectively. Moreover, the PDP of this device was improved by about 95% and 90% in comparison with SFT-FF [14] and ULPFF [7], respectively. The unique characteristics of CNTFET technology allow decrement in size of FETs to even lower than 10 nm. Therefore, this structure would be useful for low-power modules and application. As future work, we are planning to implement this structure using industry model.

References

[1] A. Karimi and A. Rezai, "Improved device performance in CNTFET using genetic algorithm," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 1, pp. 9–12, 2017.

[2] A. Karimi and A. Rezai, "A design methodology to optimize the device performance in CNTFET," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 8, pp. 1–6, 2017.

[3] M. Shafizadeh and A. Rezai, "Improved device performance in a CNTFET using La_2O_3 high k dielectrics," *Springer, J. Comput. Electron.*, vol. 16, no. 2, pp. 221–227, 2017

[4] R. W. Keyes, "The impact of Moore's law," *IEEE Solid-State Circuits Soc. Newslett.*, vol. 11, no. 3, pp. 25–27, Sep. 2006.

[5] K. Chen, "A 77% energy saving 22-transistor single phase clocking Dflipflopwithadoptive-couplingconfigurationin40nmCMOS,"in*Proc.IEEE Int. Solid-State Circuits Conf.*, Nov. 2011, pp. 338–339.

[6] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional push-pull pulsed latch with 726 fJops energy delay product in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2012, pp. 482–483.

[7] A. Karimi, A. Rezai, and M. M. Hajhashemkhani, "A novel design for ultra-low power pulse-triggered D-flip-flop with optimized leakage power," *Integr., VLSI J.*, vol. 60, no. 1, pp. 160–166, 2017.

[8] F. Klass *et al.*, "A new family of semidynamic and dynamic flip-flops with embedded logic for high-performance processors," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.

[9] V. Stojanovic and V. Oklobdzija, "Comparative analysis of master-slave latchesandflip-flopsforhigh-performanceandlow-powersystems,"*IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[10] M. Alioto, E. Consoli, and G. Palumbo, "General strategies to design nanometerflip-flopsintheenergy-delayspace,"*IEEETrans.CircuitsSyst.*, vol. 57, no. 7, pp. 1583–1596, Jul. 2010.

[11] D. M. Harris and N. H. E. West, "Circuit design of latches and flip-flops," in *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. New York, NY, USA: Addison-Wesley, pp. 392–402, Mar. 2010.

[12] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J. Sullivan, andT.Grutkowski,"TheimplementationoftheItanium2microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1448–1460, Nov. 2002.

[13] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Low power single- and double-edge-triggered flip-flops for high speed applications," *IEE Proc. Circuits Devices Syst.*, vol. 152, no. 2, pp. 118–122, 2005.

[14] J. F. Lin, "Low-power pulse-triggered flip-flop design based on a signal feed-through scheme," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 1, pp. 181–185, Jan. 2014.

[15] W. T. Chang, Ch. T. Shih, J. L. Wu, Sh. W. Lin, L. G. Cin, and W. K. Yeh, "Back-biasing to performance and reliability evaluation of UTBB FDSOI, bulk FinFETs, and SOI FinFETs," *IEEE Trans. Nanotechnol.*, vol. 17, no. 1, pp. 36–40, Jan. 2018.

[16] Ch. L. Yu, Ch. H. Yu, and P. Su, "Theoretical investigation of DIBL characteristics for scaled Tri-Gate InGaAs-OI n-MOSFETs including sensitivity to process variations," *IEEE J. Electron Devices Soc.*, vol. 5, no. 1, pp. 45–52, Jan. 2017.

[17] R. Marani and A. G. Perri, "A comparison of CNTFET models through the design of a SRAM cell," *ECS J. Solid State Sci. Technol.*, vol. 5, no. 10, pp. 118–126, 2016.

[18] A. Pacheco-Sanchez *et al.*, "Feasible device architectures for ultrascaled CNTFETs," *IEEE Trans. Nanotechnol.*, vol. 17, no. 1, pp. 100–107, Jan. 2018.

[19] C. T. Dekker, J. Sander, and A. R. M. Verschueren, "Room-temperature transistor based on a single carbon nanotube," *Nature*, vol. 393, pp. 49–52, 1998.

[20] A. Naderi, "Double gate graphene nanoribbon field effect transistor with electrically induced junctions for source and drain regions," *J. Comput. Electron.*, vol. 15, pp. 347–357, 2016.

[21] S.Lin,Y.B.Kim,andF.Lombardi,"Designofaternarymemorycellusing CNTFETs,"*IEEETrans.Nanotechnol.*,vol.11,no.5,pp.1019–1025,Sep. 2012.

[22] M. Moghaddam, M. H. Moaiyeri, and M. Eshghi, "Design and evaluation of an efficient Schmitt trigger-based hardened latch in CNTFET technology," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 1, pp. 267–277, Mar. 2017.

[23] G. Sundararajan and C. Winstead, "CNTFET-RFB: An error correction implementation for multi-valued CNTFET Logic," in *Proc. IEEE 46th Int. Symp. Multiple-Valued Logic*, 2016, pp. 11–16.

[24] N. Patil, J. Deng, S. Mitra, and H. S. P. Wong, "Circuit-level performance benchmarking and scalability analysis of carbon nanotube transistor circuits," *IEEE Trans. Nanotechnol.*, vol. 8, no. 1, pp. 37–45, Jan. 2009.

[25] R. Marani, G. Gelao, and A. G. Perri, "Modelling of carbon nanotube field effect transistors oriented to SPICE software for A/D circuit design," *Microelectron. J.*, vol. 44, no. 1, pp. 33–39, 2013.

[26] G. Gelao, R. Marani, L. Pizzulli, and A. G. Perri, "A model to improve analysis of CNTFET logic gates in Verilog-A-Part I: Static analysis," *Current Nanoscience*, vol. 11, no. 4, pp. 515–526, 2015.

[27] J. Deng and H. S. Philip Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: Full device model and circuit performance benchmarking," *IEEE Trans. Electron Device*, vol. 54, no. 12, pp. 3195–3205, Dec. 2007.

[28] S. Taghipour and R.N. Asli, "Aging comparative analysis of highperformance FinFET and CMOS flip-flops," *Microelectron. Rel.*, vol. 69, pp. 52–59, 2016.

[29] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low-power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484, May 2004.

[30] J. Deng, "Device modeling and circuit performance evaluation for nanoscaledevices:Silicontechnologybeyond45nmnodeandcarbonnanotu befieldeffecttransistors,"*Ph.D.dissertation*,StanfordUniv.,Stanford, CA, USA, 2007.

[31] J.Tschanz,S.Narendra,Z.Chen,S.Borkar,M.Sachdev,andV.De,"Comparat ive delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors," in *Proc. Int. Symp. Low Power Electron. Des.*, 2001, pp. 207–212.

[32] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra lowpower clocking scheme using energy recovery and clock gating," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 1, pp. 33–44, Jan. 2009.

[33] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low-power pulse-triggered flipflop design with conditional pulse-enhancement scheme," *IEEE*

Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 361–366, Feb. 2012.

[34] D. Markovic, B. Nikolic, and R. W. Brodersen "Analysis and design of low-energyflip-flops,"in*Proc.Int.Symp.LowPowerElectron.Des.*,2001, pp. 52–55.

[35] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *Proc. IEEE Int. Solid-State Circuits Conf. Digest Tech. Papers*, 1996, pp. 138–139.

Authors' photographs and biographies not available at the time of publication.